Amendments to the Specification:

Please replace paragraphs [0003]-[0005], [0007]-[0008], [0012], and [0035]-0042] with the following rewritten paragraphs:

[0003] In above cases, however, ~~the phenomenon of~~ power bounce or ground bounce is likely to occur. Since the number or the pad width of the power pins is reduced, the power supply is limited. When a lot of output signals of the output devices in the chip are simultaneously switched to high electric levels, there would be no sufficient power supply for the level switching operations. Therefore, a jumping and unstable phenomenon in the output signal occurs, which is so-called as "power bounce". Therefore, the electric level of the output signal from the output device will continuously toggle, resulting in possible errors of another chip electrically connected to the output end of the present chip.

[0004] Likewise, when the number or the pad width of the ground pins is not great enough or the distance between pins is too small, "ground ~~bouce~~bounce" may also occur. It is ~~becasue~~because the toggling action of an output signal will affect the electric level of an adjacent output signal via the ground pin so as to result in a continuous toggle phenomenon. The continuous toggle phenomenon is even significant when a plurality of adjacent output devices are simultaneously switched to the ground state. Under this circumstance, the ~~gound~~ground pin itself will be jumping and unstable so as to result in ground bounce. The power/ground bounce, if occurs, will adversely affects the output stability of the chip.

[0005] Please refer to Fig. 1 which is a diagram showing the waveform associated with exemplified output devices of a chip. The signal bounces of the output signals from the output devices and the ground signal at the grounding line are shown. As shown in the upper part of Fig. 1, a chip C includes output devices CQ1 and CQ2 with CMOS structures. The output device CQ1 includes transistors Q11 and Q12, and is electrically connected to an output pad (pad1) by an output end thereof. The output device CQ2 includes transistors Q21 and Q22, and is electrically connected to an output pad (pad2). ~~Further, a~~ A grounding line VSSO provides the grounding path of the output devices CQ1 and CQ2.

[0007] For solving the above power-bounce or ground-bounce problems, lots of attempts have been made, which include enhancing the driving capability of the chip by increasing the number or pad width of power pins, introducing interleaving driving operations by adding delay gate(s) so as to avoid simultaneously active high or active low status, increasing the slew rate of the electric level toggle, or enlarging the clearance between the output devices. ~~Unfortunately,~~ The above means still suffers from some problems. For example, the chip size ~~is~~ will be inevitably increased or the chip design is ~~hardly feasible~~ impractical due to high ~~operation~~ operating frequency ~~accordingly~~.

[0008] A terminator structure conventionally used for solving the signal reflection problem resulting from rapid signal transmission may have a little effect on solving the signal bounce problem. Please refer to Fig. 2 which is a schematic diagram illustrating the terminator structure. In this structure, ~~pins, e.g.~~ pins P1, P5 and Pn among the output pins P1~Pn of the chip C, are connected to a resistor R1 and a diode D1, a resistor R5 and a diode D5, and a resistor Rn and a diode Dn, respectively. The resistors R1, R5 and Rn are connected to a power source +Vcc. This structure, although solving some signal bounce problem, cannot solve the power/ground bounce problem. It is because this terminator structure can work well to inhibit signal bounce only under stable power/ground signals.

[0012] A further object of the present invention is to provide a method for ~~providing~~ optionally ~~toggled~~ toggling internal signals from a first chip to a second chip to inhibit power/ground bounce.

[0035] Please refer to Fig. 3A which shows a chip architecture according to the present invention. A first chip C1 is coupled to a second chip C2 and provides a plurality of internal signals S for the second chip C2. A signal bounce inhibiting device comprising an electric level toggling circuit 31 arranged in the output stage of the first chip C1 and an electric level recovering circuit 32 arranged in the input stage of the second chip C2. The states of the internal signals are monitored. When more than a predetermined threshold number of the internal signals

are simultaneously switched to high electric levels or low levels, signal bounce may ~~be generated~~ occur. Thus the function of the signal bounce inhibiting device is activated to toggle a selected portion of the internal signals so as to reduce the number of the internal signal switching simultaneously.

[0036] In order to toggle the internal signals S, a set of toggling control signals T are asserted and inputted to the electric level toggling circuit 31. The set of toggling control signals T includes first toggling control signals controlling selected ones of the internal signals S to toggle, and second toggling control signals controlling the other ~~ones of the~~ internal signals not to toggle. In response to the toggling control signals T, the internal signals S are transmitted to and processed by the electric level toggling circuit 31 to obtain different output signals St, i.e. some of the output signals St are toggled and the others remain unchanged. The output signals St then enter the electric level recovering circuit 32 in the second chip C2 to be further processed. In the second chip C2, a set of recovering control signals R are asserted and inputted to the electric level recovering circuit 32. The set of recovering control signals R correlate to and vary with the set of toggling control signals T. Accordingly, corresponding to the first and second toggling control signals, first and second recovering control signals are included in the set of recovering control signals R, and what parts of the output signals St should be recovered by the electric level recovering circuit 32 can be determined in response to the first recovering control signals. Preferably, the set of recovering control signals R and the set of toggling control signals T are identical and asserted by the same CPU 33. In other words, upon the internal signals S are transmitted from the first chip C1 to the second chip C2, the toggling and recovering control signals T and R are provided for the first and the second chips C1 and C2, respectively. In response to the first recovering control signals, the toggled ones of the output signals St are recovered into the internal signals S, while in response to the second recovering control signals, the unchanged ones of the output signals St still remain unchanged. The details relating to how the electric level toggling circuit 31 and the electric level recovering circuit 32 work will be described hereinafter.

[0037] Please refer to Fig. 3B, in which a preferred embodiment of the signal bounce inhibiting device according to the present invention is illustrated. The electric level toggling circuit 31

includes N electric level toggling units 311, 312,..., 31n, and the electric level recovering circuit 32 includes N electric level toggling units 321, 322,..., 32n. Each pair of the electric level toggling and recovering units process one of the N internal signals S1~Sn. In this embodiment, the ~~count~~ number of the electric level toggling units 311~31n or electric level recovering units 321~32n is equal to the total ~~count~~ number of the internal signals S1~Sn to be provided from the first chip C1 to the second chip C2.

[0038] Preferably, the set of recovering control signals R and the set of toggling control signals T are ~~generated by~~ determined after a series of test procedures. By providing various tested control signals, the simultaneous switching output (SSO) degrees in the chip system are observed. The test results are recorded in the system, e.g. in an optical recording and reproducing system. Then, according to practical applications, suitable toggling and recovering control signals are provided for the first and the second chips, respectively, to perform the signal bounce inhibiting operations as mentioned above. On the basis of the test results, the pins never to be toggled in response to the toggling control signals are known. For these pins, no electric level toggling units are required. Therefore, the electric level recovering units as well as the electric level toggling units can be omitted for cost and chip-size reduction. The elements ~~showing~~ shown in Fig. 3B can be used ~~are applied hereto~~ to illustrate ~~this~~ the embodiment that some ~~of the pins are omitted from coupling thereto~~ electric level toggling and recovering units are omitted.

[0039] In this embodiment, more than N internal signals S, for example M internal signals, are to be provided from the first chip C1 to the second chip C2. ~~, for example~~ The M internal signals~~, are internal signals S1~Sn,~~ are processed by the signal bounce inhibiting device of the present invention~~. Accordingly~~, but only the internal signals S1~Sn are transmitted through the electric level toggling units 311, 312,..., 31n and electric level recovering units 321, 322,..., 32n to be processed according to the present invention. It is to be noted that the internal signals S1~Sn in this alternative embodiment do not have to be immediately adjacent to one another. The numbers 1~n just indicate N ones among the M internal signals are processed rather than imply the continuity of the N internal signals. The electric level toggling and recovering units are arranged according to the test results stored in the system drive.

[0040] In both of the above embodiments, it is preferred that the electric level toggling units 311, 312,..., 31n include respective registers TC1, TC2,..., TCn, and XOR gates TX1, TX2,..., TXn. Likewise, the electric level toggling units 311, 312,..., 31n include respective registers RC1, RC2,..., RCn, and XOR gates RX1, RX2,..., RXn. When it is determined that ~~too~~ many internal signals are switching their states at the same time, the toggling control signals T1, T2,..., Tn are inputted and stored into the registers TC1, TC2,..., TCn, respectively. Some of the toggling control signals T1, T2,..., Tn~~, which~~ are at high levels to serve as the first toggling control signals, ~~which are,~~ and the others are ~~made~~ at low levels to serve as the second toggling control signals. The XOR gates TX1, TX2,..., TXn receive corresponding internal signals S1, S2,..., Sn and toggling control signals T1, T2,..., Tn from the registers TC1, TC2,..., TCn, respectively, and perform XOR operations on those signals to obtain output signals St1, St2,..., Stn. ~~Therefore, for~~ For those XOR gates that receive the first toggling control signals ~~at~~, i.e. high levels, the internal signals are toggled to obtain output signals with changed electric levels. On the other hand, for those XOR gates that receive the second toggling control signals at low levels, the internal signals are not toggled so as to obtain output signals without electric level change. ~~By~~In this way, the number of internal signals ~~that are simultaneously~~ changing their states simultaneously can be reduced so as to inhibit the signal bounce, e.g. power/ground bounce.

[0041] After the internal signals S1, S2,..., Sn are processed into the output signals St1, St2,..., Stn by the electric level toggling circuit 31 in the first chip C1, and provided for the second chip C2, the output signals St1, St2,..., Stn should be recovered to the original internal signals S1, S2,..., Sn by the electric level recovering circuit 32. The recovering control signals R1, R2,..., Rn ~~including the first and the second recovering control signals~~ are inputted and stored into the registers RC1, RC2,..., RCn, respectively. Some of the recovering control signals R1, R2,..., Rn are at high levels and serve as the first recovering signals, and the others are ~~made~~ at low levels and serve as the second recovering control signals. The XOR gates RX1, RX2,..., RXn receive corresponding output signals St1, St2,..., Stn and recovering control signals R1, R2,..., Rn from the registers RC1, RC2,..., RCn, respectively, and perform XOR operations on those signals to ~~obtain recovered~~ recover signals S1, S2,..., Sn. ~~Therefore, for~~ For those XOR gates that receive

the recovering control signals at high levels, the electric levels of their ~~the~~ output signals will change ~~change their electric levels to be recovered to the internal signals~~. On the other hand, for those XOR gates that receive the recovering control signals at low levels, the electric levels of ~~the~~ their output signals will not change. In other words, some of the output signals St1, St2,..., Stn, which previously changed electric states thereof in response to the first toggling control signals, changes their electric states again in response to the first recovering control signals, while the other output signals St1, St2,..., Stn, which had their electric states remain unchanged in response to the second toggling control signals, still remain unchanged in response to the second recovering control signals. Accordingly, all the signals output signals St1, St2,..., Stn can be recovered to the internal signals S1, S2,..., Sn~~, which have not been toggled previously, are not changed so that the corresponding original internal signals corresponding original~~.

[0042] According to the present invention, the signal bounce can be inhibited by properly toggling some of the signals ~~on~~ simultaneously changing to high electric levels or low levels. Further, since the toggling operations can be performed on selected internal signals, it is very flexible for various chip architectures.